Product News

Date: November 16, 2022

Smaller Code, Higher Performance: Latest IAR Embedded Workbench for RISC-V Leverages CoDense™ from Andes

IAR Embedded Workbench for RISC-V v3.11 and Andes CoDense™ extension of the AndeStar™ V5 RISC-V processors help embedded developers to shrink their code size and increase their applications' performance.

Uppsala, Sweden – November 16, 2022 – IAR Systems®, the world leader in software and services for embedded development, has just announced the full support of their latest release of IAR Embedded Workbench for RISC-V for the CoDense™ extension of Andes Technology's AndeStar™ V5 RISC-V processor. CoDense™ is a patented extension of the processor's ISA (Instruction Set Architecture) which helps IAR's toolchain to generate a compact code – for saving flash memory on the target processor while the previously supported AndeStar™ V5 DSP/SIMD and Performance extensions help deliver higher application performance. IAR Systems has already supported the AndesCore™ RISC-V CPU IP at an early stage, offering customers a complete development toolchain including the powerful IAR C/C++ Compiler™ and a comprehensive debugger, which is also available in an ISO 26262 conforming functional safety certified edition.

Andes is a founding Premier member of RISC-V International and a leading supplier of high-performance/low-power 32/64-bit embedded processor IP solutions. The joint solutions from Andes and IAR Systems with their robust design methodology for safety applications help customers accelerating development including the certification process and therefore their products' time to market. CoDense™ in AndeStar™ V5 is an Andes-extended feature for code size compression on top of the extensible RISC-V standard instructions. The extension has already been proven in more than 10 billion SoCs with AndeStar™ V3 processors. Besides the support for CoDense™, the latest version 3.11 of the IAR Embedded Workbench for RISC-V comes with a "P" extension 0.9.11 support (Standard Extension for Packed-SIMD Instructions) and enhanced SMP (Symmetric Multi-Processing) and AMP (Asymmetric Multi-Processing) multicore debugging. Developers will also appreciate the new IAR Build and IAR C-SPY Debug extensions for Visual Studio Code, so they can utilize IAR Systems' powerful tools for building and debugging their code within the Visual Studio Code editor.

The proven IAR Embedded Workbench is on the rise among RISC-V developers with its best-in-class code size optimizations, which allows companies to use smaller devices or add even more functionality

– more –

to an existing platform. The code is generated using the toolchain's advanced optimization technology and convinces in CoreMark tests from the EEMBC Certification Lab with its fast code and industry-leading performance. The included C-SPY Debugger gives developers full control of the application in real-time, amongst others by using complex breakpoints, profiling, code coverage, timeline with interrupt, and power logging. Fully integrated code analysis tools ensure compliance with specific standards like MISRA C (2004 and 2012) as well as the best programming practices like Common Weakness Enumeration (CWE) and CERT C Secure Coding Standard. Being certified for functional safety development itself, the IAR Embedded Workbench for RISC-V comes with a safety report and safety guide for ten different standards, e.g. for automotive or industrial applications.

"We are glad that IAR Systems provides full support to AndeStar™ V5 RISC-V processors, especially including the enhancement of the patented CoDense™ extension in this release," said Dr. Charlie Su, President and CTO of Andes Technology. "CoDense™ increases the code density significantly by double digits and is very welcome in MCU or IoT applications. We look forward to the competitive combination of IAR Embedded Workbench with AndeStar™ V5 RISC-V extensions with up to 30 percent higher performance made available to the RISC-V community."

"Thanks to our close cooperation with Andes, we provided early support for the AndeStar™ V5 DSP/SIMD and Performance extensions and now full support for Andes CoDense™, enabling code size compressions on top of RISC-V C-extension," said Anders Holmberg, CTO at IAR Systems. "The balance between code size and performance can make a real difference for total return on investment from a product or project. With CoDense™ support, we give our users the power to tip this balance in their favor."

For more information on the IAR Embedded Workbench for RISC-V, the functional safety-certified edition of the tool suite, and IAR Systems' overall offering for RISC-V, please visit https://www.iar.com/riscv.

Ends

IAR Systems Contacts

Rafael Taubinger, Senior Product Marketing Manager, IAR Systems
Tel: +46 18 16 78 00 Email: rafael.taubinger@iar.com

About IAR Systems

IAR Systems provides world-leading software and services that drive developer productivity in embedded development and embedded security, enabling companies worldwide to create and secure the products of today and the innovations of tomorrow. IAR Systems' tools support more than 15,000 devices from

over 200 semiconductor partners worldwide, serving some 100,000 developers, who are working for a mix of Forbes 2000 companies, SMEs, and startups. IAR Systems is headquartered in Uppsala, Sweden, and has more than 220 employees in 14 offices distributed across APAC, EMEA, and North America. IAR Systems is owned by I.A.R. Systems Group AB, listed on NASDAQ OMX Stockholm, Mid Cap (ticker symbol: IAR B). Learn more at www.iar.com.